

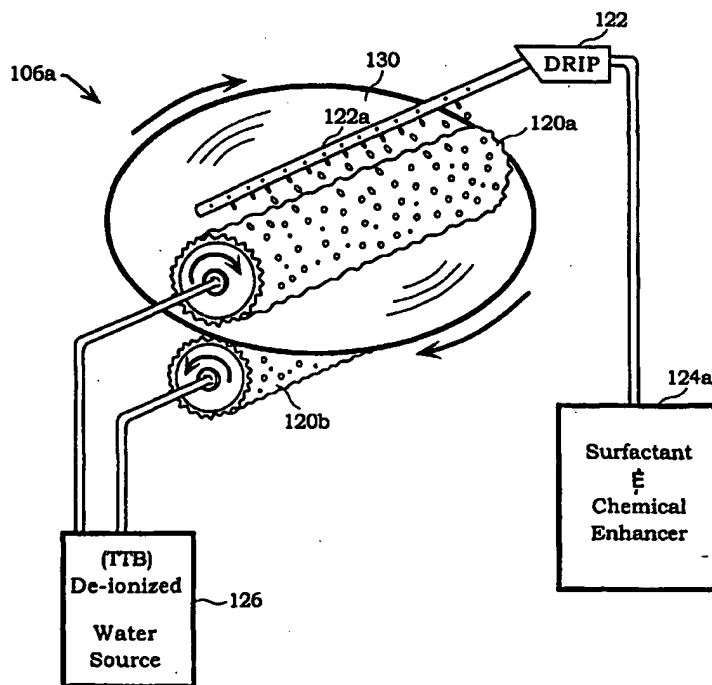


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(54) Title: METHOD AND APPARATUS FOR CLEANING LOW K DIELECTRIC AND METAL WAFER SURFACES**(57) Abstract**

Disclosed is a method for cleaning hydrophobic surfaces, such as low K dielectric organic or inorganic surfaces as well as metallization surfaces of a semiconductor wafer. The method includes: (a) applying a surfactant solution to the surface; (b) scrubbing the surface; and (c) spin-rinsing the surface of the substrate using de-ionized water to complete a removal of any contaminants from the surface. If needed, the surfactant solution can be mixed with a chemical enhancer, and the scrubbing can be performed in a brush system. The brush system may be configured to apply DI water using a through the brush (TTB) technique. The surfactant solution can be applied either using a drip technique or using the TTB technique.



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METHOD AND APPARATUS FOR CLEANING LOW K DIELECTRIC AND METAL WAFER SURFACES

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to the cleaning of semiconductor wafers, and, more particularly, to techniques for cleaning wafers having hydrophobic low k dielectric and metal surfaces.

2. Description of the Related Art

Integrated circuits utilize dielectric layers to insulate conductive lines on various layers of a semiconductor structure. However, as circuits become faster and more compact, the distances between the conductive lines decrease, which necessarily introduces increased coupling capacitance. Therefore, it has become increasingly important to have a dielectric layer that is able to better insulate conductive lines against the increasing coupling capacitance levels, which have the drawback of slowing the operation of the semiconductor device.

Figure 1A is a cross-sectional view illustrating several layers of a typical prior art integrated circuit 10. The integrated circuit 10 includes a substrate 12 that supports an oxide dielectric layer 14, which is typically silicon dioxide (SiO_2). A metal layer typically made of aluminum (Al) is deposited onto the oxide dielectric layer 14 and etched into a plurality of metal lines 16. For ease of illustration, only two metal lines 16 are shown, but as is well known in the art, many additional metal lines 16 are used to provide the necessary interconnections of a layer of an integrated circuit device.

Generally, the coupling capacitance in an integrated circuit is directly proportional to the dielectric constant (K) of the dielectric material used. The oxide dielectric layer 14, which is typically made from silicon dioxide, has a dielectric constant of about 4.0. Because line

densities and operating frequencies in semiconductor devices are constantly increasing, the coupling capacitances between conductive lines have increased to the point that the oxide dielectric layer 14 having a dielectric constant of about 4.0 is a less than adequate insulator.

Figure 1B is a cross-sectional view illustrating several layers of another type of prior art integrated circuit 20 incorporating an organic dielectric layer 22. The organic dielectric layer 22 typically has a dielectric constant of between about 1.5 and about 3.5. Thus, the organic dielectric layer 22 is much less conductive than the oxide dielectric layer 14 and better able to isolate conductive lines and reduce the coupling capacitances. After the organic dielectric layer 22 is formed over the substrate 12, a plurality of trenches 24 is etched into the organic dielectric layer 22. Then, the trenches 24 are filled by depositing a copper (Cu) layer 26 (or aluminum) over the organic dielectric layer 22.

Figure 1C illustrates the integrated circuit 20 of Figure 1B after a conventional chemical mechanical polishing (CMP) operation is performed. The CMP process planarizes the top surface of the copper layer 20 down to the organic dielectric layer 22 and the resulting copper lines 28. However, the CMP process leaves behind a film of particles and metal contaminants ("contaminants") 30 on the surface of the dielectric layer 22 and the copper lines 28. As is well known in the art, copper has a lower resistance than the aluminum used in the integrated circuit 10 of Figure 1A. However, copper is also known to be more susceptible to corrosion than aluminum, which makes it even more important to clean contaminants 30 from its surface.

Figure 1D illustrates another partial view of a prior art semiconductor device 40 where the organic dielectric layer 22 is spun on or deposited by chemical vapor deposition (CVD). Figure 1E illustrates another partial view of a prior art semiconductor device 50 after a via hole 52 is etched through a dielectric layer 54 down to a metal line 56. In both the semiconductor devices 40 and 50, the spin-on/deposition and via hole etch leave behind a film of contaminants 30.

In the integrated circuit 10 of Figure 1A, any particles were capable of being cleaned by simply, *e.g.*, spraying the surface of the oxide dielectric layer 14 with aqueous solutions such as de-ionized water, or de-ionized water and acid/base. As is well known, cleaning the particles from the surface of silicon dioxide type dielectrics is rather straight forward because this kind of material is substantially hydrophilic. That is, when cleaning fluids are applied to

the surface of a hydrophilic material, the fluids will actually wet over the surface. To further facilitate cleaning, some cleaning processes implement a special polyvinyl alcohol (PVA) brush (*i.e.*, a very soft sponge) to assist in dislodging the particles, using de-ionized water and/or acid/base. The particles would then be removed from the surface of the silicon oxide dielectric layer when rinsed off.

Unfortunately, this conventional method of cleaning the semiconductor wafer does not work for semiconductor devices that incorporate low K dielectric polymers and/or organic dielectric materials, such as the organic dielectric layer 22. Organic dielectric materials are hydrophobic, therefore, the cleaning fluids are repelled from the surface of the organic materials. As is well known, a contact angle may be measured from a droplet of water that is in direct contact with a given material to determine the degree of repulsion.

In addition, organic dielectric materials are chemically inert, which prevent them from reacting with chemical reagents to convert hydrophobic surfaces into hydrophilic surfaces while leaving the bulk materials intact. Because standard cleaning fluids fail to achieve sufficient contact with the hydrophobic organic dielectric materials, scrubbing the semiconductor wafer with a brush would only draw more particles to the surface of the wafer. Therefore, using scrubbing techniques over hydrophobic organic surfaces will only exacerbate the particle contamination problem. As is well known, some hydrophobic organic surfaces can be cleaned using organic solvents. However, such organic solvents are often highly toxic and more expensive than water. Further yet, when the toxic organic solvents are used, more complex equipment is required to perform the cleaning processes. The brush material, PVA, is, in general, not compatible with organic solvents. As a result, cleaning using organic solvents is highly undesirable.

In view of the foregoing, it is desirable to have an apparatus and method of cleaning particles and/or metal contaminants from hydrophobic organic dielectric layers using aqueous solutions without damaging the integrated circuit surface.

SUMMARY OF THE INVENTION

The present invention fills these needs by providing an efficient and economical method and apparatus for cleaning low K dielectric polymer surfaces (organic and inorganic) and metallization surfaces of a wafer without damaging the integrated circuit device surface.

It should be appreciated that the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, a device or a method. Several inventive embodiments of the present invention are described below.

In one embodiment of the present invention a method for cleaning a low K dielectric
5 film surface of a semiconductor substrate is disclosed. The method includes applying de-ionized water and a surfactant formulation solution to the low K dielectric polymer surface to form a wettable conditioning layer. The wettable conditioning layer is configured to commence the cleaning that is targeted to remove particle and/or metal contaminants throughout the low K dielectric polymer surface. To continue the cleaning, de-ionized water
10 and a surfactant solution are applied over the low K dielectric polymer surface. The semiconductor substrate then is spin-rinsed to remove any applied surfactant formulation solution or surfactant solution while removing the remaining particle contaminants and/or metal contaminants from over the low dielectric polymer surface.

In another embodiment of the present invention an alternative method for cleaning a
15 low K dielectric film surface of a semiconductor wafer is disclosed. The method includes applying a first mixture of de-ionized water and a surfactant formulation solution to the organic dielectric surface, and then scrubbing the organic dielectric surface. A second mixture of de-ionized water and a surfactant solution is then applied to the dielectric surface, and subsequently scrubbed to continue the cleaning. The substrate is then spin-rinsed using
20 de-ionized water to complete a removal of any contaminants from the organic dielectric surface.

In yet another embodiment of the present invention, an apparatus for cleaning an organic dielectric surface of a semiconductor wafer is disclosed. The apparatus includes a first cleaning stage for applying a first mixture of de-ionized water and a surfactant
25 formulation solution to the dielectric surface. The first cleaning stage incorporates a first brush system for scrubbing the dielectric surface using the first mixture. The apparatus includes a second cleaning stage for applying a second mixture of de-ionized water and a surfactant solution to the dielectric surface. The second cleaning stage incorporates a second brush system for scrubbing the organic surface using the second mixture. After the second
30 cleaning stage is complete, a spin-rinsing bowl is used for rinsing the wafer using de-ionized water to complete a removal of any contaminants from the dielectric surface.

Still further, in another embodiment, a method for cleaning a surface of a semiconductor substrate is disclosed. In this embodiment, the surface can be one an low K dielectric, an inorganic low K dielectric, an aluminum metallization, or any combination thereof. Therefore, in this embodiment, the method includes applying de-ionized water and a surfactant formulation solution to the surface to form a wettable conditioning layer. The
5 applying is configured to commence the cleaning that is targeted to remove particle contaminants and metal contaminants throughout the surface. The method then proceeds to applying de-ionized water and a surfactant solution over the surface to continue the cleaning. In a modification of this embodiment, the surfactant solution can be converted into a
10 surfactant formulation solution by simply adding a chemical enhancer. Next, the method will move to spin-rinsing the semiconductor substrate to remove any applied surfactant formulation solution or surfactant solution while removing any remaining particle contaminants and/or metal contaminants from over the surface.

In still another embodiment, the method for cleaning a surface of a hydrophobic
15 substrate of a semiconductor wafer is disclosed. The method includes: (a) applying a surfactant solution to the surface; (c) scrubbing the surface; and (c) spin-rinsing the surface of the substrate using de-ionized water to complete a removal of any contaminants from the surface. If needed, the surfactant solution can be mixed with a chemical enhancer, and the scrubbing can be performed in a brush system. The brush system is thus configured to apply
20 DI water using a through the brush (TTB) technique. In this embodiment, the surfactant solution can be applied either using a drip technique or even using the TTB technique.

An advantage of the present invention is that it provides for the temporary wetting of hydrophobic surfaces to achieve excellent cleanability. More specifically, the present invention allows the cleaning of the many types of hydrophobic dielectric materials in
25 semiconductor wafers including low K dielectric polymers, organic materials, inorganic materials, and conductive materials (i.e., metals).

Because semiconductor manufacturing is a very precise art, maintaining clean surfaces in all phases of fabrication is extremely important. Hydrophobic dielectric layers are known to accumulate a large amount of microscopic particles and/or metal contaminants during and
30 after processes such as chemical vapor deposition (CVD), via hole etching, and chemical mechanical polishing (CMP). Therefore, it is extremely important to remove the particle

contaminants, not only to fabricate a semiconductor device that conforms to its intended specifications. Furthermore, the embodiments of the present invention also enable, among other suitable techniques, the use of scrubber-based cleaning technologies to hydrophobic low K film cleaning.

5 Other aspects and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

10 The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements.

Figure 1A is a cross-sectional view illustrating several layers of a typical prior art integrated circuit.

15 Figure 1B is a cross-sectional view illustrating several layers of another type of prior art integrated circuit incorporating an organic dielectric layer.

Figure 1C illustrates the integrated circuit of Figure 1B after a conventional CMP operation is performed.

Figure 1D illustrates another partial view of a prior art semiconductor device where the organic dielectric layer is spun on or deposited by CVD.

20 Figure 1E illustrates another partial view of a prior art semiconductor device after a via hole is etched through a dielectric layer down to a metal line.

Figure 2A shows a wafer cleaning station of the present invention that may be controlled in an automated way by a cleaning control station.

Figure 2B shows a more detailed schematic of the exemplary wafer cleaning station.

25 Figure 2C shows a detailed view of the cleaning process performed in the first cleaning stage in accordance with one embodiment of the present invention.

Figure 2D shows the chemical application technique used in both the first cleaning stage and the second cleaning stage.

Figure 2E shows a detailed view of the cleaning process performed in the second cleaning stage in accordance with one embodiment of the present invention.

5 Figure 3A shows a more detailed cross sectional view of a contaminated semiconductor wafer beginning the cleaning with surfactant solutions in accordance with one embodiment of the present invention.

Figure 3B is a more detailed view of the contaminated surface of the low K dielectric polymer layer.

10 Figure 3C shows the semiconductor wafer substantially free of particle contaminants and the applied cleaning solutions.

Figure 4 is a flow chart illustrating a method of cleaning a wafer having a hydrophobic surface in accordance with one embodiment of the present invention.

15 Figure 5 is a more detailed flow chart diagram of a method of cleaning a wafer having a hydrophobic surface in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

20 A method and apparatus for cleaning low K dielectric materials and metallization materials on wafers is disclosed. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be understood, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

25 Figure 2A shows a wafer cleaning station 100 of the present invention that may be controlled in an automated way by a cleaning control station 102. The wafer cleaning station 100 includes a sender station 104, a cleaning stage 106, a spin-rinse and dry (SRD) station 108, and a receiver station 110. As will be described below in, the cleaning techniques of the present invention are advantageously run at room temperature, which greatly simplifies the

equipment of the cleaning station 100.

As a broad overview of the cleaning process, contaminated semiconductor wafers are initially placed into the sender station 104. The sender station 104 then delivers a wafer (one-at-a-time) to the cleaning stage 106 where a low K dielectric hydrophobic surface of the wafer is conditioned to enable particles and/or metal contaminants to be efficiently removed from the surface.

In one embodiment, the cleaning stage 106 is preferably divided into a first cleaning stage 106a and a second cleaning stage 106b, although having just one cleaning stage 106 may also work. Having two cleaning stages 106a and 106b allows the wafer cleaning station 100 to apply two types of cleaning/conditioning solutions to the wafer. Preferably, during a cleaning cycle, each wafer spends between about 30 seconds and about 45 seconds, and more preferably about 35 seconds in each cleaning stage 106a and 106b. After passing through the cleaning stage 106, the wafer is passed through an exit spray in order to remove the cleaning/conditioning solutions and any contaminants. The spin-rinse is performed to enable the final cleaning of leftover particle contaminants and cleaning/conditioning solution. Then the SRD station 108 dries the wafer. Finally, the wafer is delivered to the receiver station 110 to be stored.

Figure 2B shows a more detailed schematic of the exemplary wafer cleaning station 100. Both the sender station 104 and the receiving station 110 are preferably adapted to receive a cassette containing a number of wafers. The first and second cleaning stages 106a and 106b preferably include a set of PVA brushes 120 that are very soft and porous. Therefore, the brushes 120 are capable of scrubbing the wafer clean without damaging the delicate surface. Because the brushes 120 are porous, they are also able to function as a conduit for fluids that are to be applied to the wafer surface..

Figure 2C shows a detailed view of the cleaning process performed in the first cleaning stage 106a in accordance with one embodiment of the present invention. In the first cleaning stage 106a, a wafer 130 is inserted between a top brush 120a and a bottom brush 120b. The wafer 130 is capable of being rotated to enable the brushes 120a and 120b to adequately clean the entire surface of the wafer 130. In certain circumstances, the bottom surface of the wafer is required to be cleaned as well, because the contaminants from the bottom may migrate to the top surface. Although both the top surface and the bottom surfaces

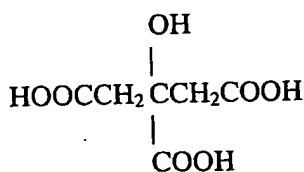
of the wafer are scrubbed with the brushes 120, the top surface that is scrubbed with the top brush 120a is the primary surface targeted for cleaning, since the top surface is where the integrated circuit devices are being fabricated.

During cleaning, a water source 126 is configured to supply de-ionized (DI) water through the brush (TTB) for both brushes 120a and 120b, using a flow of about 200 to about 1000 mL/minute, and more preferably about 500 mL/minute onto the wafer 130. A drip chemical applicator 122 is positioned above the top brush 120a to allow an application arm 122a to drip a surface active reagent (surfactant) formulation solution 124a onto the top brush 120a. The surfactant formulation solution 124a is preferably dripped at a flow rate of about 150 to about 250 mL/minute. In an alternative embodiment, the chemicals can also be delivered through the brush (TTB) as opposed to drip delivery.

Figure 2D shows the chemical application technique used in both the first cleaning stage 106a and the second cleaning stage 106b. In the first cleaning stage 106a, after the surfactant formulation solution 124a is dripped onto the top brush 120a, it mixes with the de-ionized water provided by the water source 126. The top brush 120a is then lowered onto the wafer 130 to scrub and clean the wafer 130. The cleaning solution is therefore made of a combination of the drip applied surfactant formulation solution 124a and the de-ionized water applied TTB as a cleaning solution.

The surfactant formulation solution 124a preferably includes surfactant and a chemical enhancer such as citric acid having the chemical formula identified in table A. Other organic acids, such as malic and acetic acids should also work well. Alternatively, the chemical enhancer may also be bases, such as a base ammonia (NH₄OH), or a mixture of citric and ammonia. Other alternative examples for the base ammonia chemical enhancer include, for example, an organic base such as an alkylammonium hydroxide. Examples of the alkylammonium hydroxide may include a tetramethylammonium hydroxide and a tetrabutylammonium hydroxide.

TABLE A



In one embodiment, the chemical enhancer is used to control an electric charge, also referred to as a zeta potential, of the top brush 120a, the hydrophobic surface of the wafer 130, and the particle contaminants. Controlling the electric charge is needed so that the same electric charge sign (positive or negative) is on the brush, wafer surface and the particles. In general, if the chemical enhancer is an acid, there is a decrease in the pH and an increase in the zeta potential. If the chemical enhancer is a base, there is an increase in the pH and an decrease in the zeta potential. The charge aids in cleaning the wafer 130 by further repelling particle contaminants away from the surface of the wafer 130. The charge also keeps the top brush 120a clean by repelling the particle contaminants away from the brush 120a, and preventing brush loading (*i.e.*, accumulation of contaminants in the brush). A mixture of citric and ammonia is used to control both zeta-potential and pH.

The surfactant is preferably a non-ionic or an anionic surfactant, and most preferably includes aromatic rings (for organic low K dielectric applications). Furthermore the chosen surfactant chemical should be capable of being easily rinsed off from the wafer surface at the end of cleaning. One example company that produces surfactants having these qualities is Valtech Corporation, of Pughtown PA. Valtech's product identifiers for the surfactants are, for example, SP 2275 and DP 93001. Preferably, the surfactant, in one embodiment, should have a concentration of about 0.1 % to about 1 % by volume of the surfactant formulation solution 124a (which includes both the surfactant and the chemical enhancer).

In the concentrations described herein, it is assumed that the concentration of the surfactant solution obtained from Valtech is 100% by volume, however, many suppliers may provide surfactant solutions with different concentrations. To achieve the preferred concentrations therefore, different diluting with de-ionized water may be performed.

If citric acid is used as the chemical enhancer, the citric acid should preferably have a concentration of about 0.1% to about 5% by weight of the surfactant formulation solution 124a. If ammonia is used, it should preferably have a concentration of about 0.02% to about 5% by weight of the surfactant formulation solution 124a. Thus, the surfactant formulation solution 124a is pre-mixed with DI water to achieve the desired concentration levels. Before the wafer 130 is moved out of the first cleaning stage 106, it is lightly rinsed with DI water through the brush (TTB) to remove the surfactant formulation solution and/or particle and

metal contaminants.

Figure 2E shows a detailed view of the cleaning process performed in the second cleaning stage 106b in accordance with one embodiment of the present invention. After the wafer 130 has been through the first cleaning stage 106a, it is transferred to the second cleaning stage 106b. The wafer 130 is again inserted between a top brush 120a and a bottom brush 120b. The wafer 130 is capable of being rotated to enable the brushes 120a and 120b to clean the entire surface of the wafer 130. A water source 126 is also capable of supplying DI water through the brush (TTB) to both brushes 120a and 120b.

A drip chemical applicator 122 is positioned above the top brush 120a to allow an application arm 122a to drip a surfactant solution 124b onto the top brush 120a and the wafer 130. Unlike the surfactant formulation solution 124a, the surfactant solution 124b preferably contains a concentration of about 0.1% to about 1% by volume surfactant, without any chemical enhancers. The top brush 120a is then lowered onto the wafer 130 to scrub and clean the wafer 130 using the combination of the surfactant solution 124b and the de-ionized water as shown in Figure 2D. As applied in the first cleaning stage 106a, the de-ionized water is preferably applied using a flow of about 200 to about 1000 mL/minute, and more preferably about 500 mL/minute.

Alternatively, if the first cleaning stage 106a was not as successful as desired in cleaning the contaminants from the surface of the wafer, the second cleaning stage 106b can also be configured to apply the chemical enhancer. If the chemical enhancer is added in the second cleaning stage 106b, the surfactant solution 124b (of Figure 2E) would essentially be replaced with the surfactant formulation solution 124a (of Figure 2C). Further yet, if the first cleaning stage 106a performs an adequate cleaning job on the material being cleaned, there may not be a need for the second cleaning stage 106b.

As still a further alternative, the cleaning of some types of surfaces may not even require the application of the chemical enhancer in either the first stage or the second stage. In such cases, both the first stage and the second stage will only apply the surfactant solution. When this is the case, there may not even be a need to two separate stages, and a single surfactant solution application stage will be implemented.

Figure 3A shows a more detailed cross sectional view of a contaminated

semiconductor wafer 130' beginning the cleaning with surfactant solutions in accordance with one embodiment of the present invention. The wafer 130' includes a substrate 132 with a low K dielectric polymer layer 134 formed over the substrate 132. The low K dielectric polymer layer 134 (e.g. an organic type material) is much less conductive than layers made from silicon dioxide. The low K dielectric polymer layer 134 typically has dielectric constant values ranging between about 1.5 and about 3.5.

Unfortunately, while the low K dielectric polymer layer 134 is a much better insulator than the silicon dioxide dielectric materials, and greatly reduces the coupling capacitance between metal lines 135, it is much harder to clean and remove particles and/or metal contaminants 138 from the surface of the low K dielectric polymer layer 134 because it is hydrophobic. As is well known in the art, a contact angle between a drop of water and the surface of a material can be measured to determine whether the material is hydrophobic or hydrophilic. Typically, a contact angle of about 20° or above generally indicates that the material is hydrophobic. Consequently, conventional water and other aqueous cleaning fluids are unable to wet the surface and rinse away particle contaminants 138 because they are repelled and bead on the surface of the low dielectric polymer layer 134.

As described above, the cleaning process of the present invention includes the use of cleaning solutions that contain surfactant. Surfactant molecules 136 are amphiphilic, containing both hydrophobic and hydrophilic groups (e.g., a hydrophilic group 136a and a hydrophobic group 136b). Thus, the hydrophobic group 136b of the surfactant molecule 136 is attracted to a hydrophobic surface. Figure 3B is a schematic representation of a surfactant molecule over the contaminated surface of the low K dielectric polymer layer 134. When surfactant is applied to the wafer, the hydrophobic group 136b attaches the surfactant molecule 136 to the low K dielectric polymer layer 134.

At the same time, the hydrophilic group 136a of the surfactant molecule 136 attracts de-ionized water and other cleaning fluids to enable the wetting of the surface of the low K dielectric polymer layer 134. Because the surface now wets, the top and bottom brushes 120a and 120b are now able to dislodge the particle and metal contaminants 138 and sweep them into the cleaning fluids by scrubbing the low K dielectric polymer layer 134. Any remaining particle contaminants 138 and the surfactant molecules 136 are then capable of being rinsed away with DI water (e.g., in the spin-rinse and dry station 108), leaving the wafer 130'

substantially free of particle contaminants 138 and the applied cleaning solutions as shown in Figure 3C.

Figure 4 is a flow chart illustrating a method 200 of cleaning a wafer having a hydrophobic surface in accordance with one embodiment of the present invention. The method 200 starts at an operation 202 by providing a substrate, which can be, for example, any type of semiconductor wafer. An operation 204 forms a hydrophobic layer over the substrate. The hydrophobic layer is designed to provide insulation for metal lines in the substrate and preferably consists of a low K dielectric polymer (i.e., organic dielectric) material. De-ionized water and a surfactant formulation solution are applied to the hydrophobic layer to make a wettable conditioning layer in an operation 206. The surfactant formulation solution preferably includes surfactant and a chemical enhancer. The wettable conditioning layer begins cleaning of particles and/or metal contaminants from the hydrophobic layer.

An operation 208 will also apply de-ionized water, but discontinues the application of the chemical enhancer used in operation 206. Instead, a surfactant solution consisting of only surfactant is applied to the substrate. During this cleaning operation, the wettable conditioning layer continues to assist in the cleaning. Next, an operation 210 spin rinses the applied solutions leaving the hydrophobic layer substantially clean of particles and/or metal contaminants. An operation 212 then dries the substrate, and an operation 214 stores the substrate. In an operation 216 it is determined whether there are any more substrates to clean. In general, the sender station starts sending a new wafer to be cleaned to the first stage 106a after the wafer that was previously in the first stage 106a has been moved to the second stage 106b. Thus, if there are more wafers to clean, then the process repeats from operation 202. If not, the method 200 ends.

Figure 5 is a more detailed flow chart diagram of a method 300 of cleaning a wafer having a hydrophobic surface in accordance with another embodiment of the present invention. The method 300 starts with an operation 302 by providing a substrate, such as a semiconductor wafer. Next, a hydrophobic layer is formed over the substrate through any suitable chemical vapor deposition (CVD) technique in an operation 304.

In operation 306, the hydrophobic layer may be planarized by chemical mechanical polishing (CMP), or a via hole etch may be performed through the hydrophobic layer. As is

well known, the CMP process will remove excess dielectric material from the hydrophobic layer, as well as excess deposited metal from any metal lines that may be formed in the hydrophobic layer. However, whether the hydrophobic surface has just been deposited, processed through a CMP operation or a via etch, contaminants will most likely be present, therefore requiring a thorough cleaning.

Operation 308 moves the substrate to a first cleaning station. There, de-ionized water is applied through a top brush and a bottom brush and a surfactant formulation solution is drip applied to the top brush in an operation 310. Cleaning is begun in an operation 312 by lowering the top brush so that it scrubs the hydrophobic layer and dislodges particle contaminants on the surface of the hydrophobic layer into the cleaning solutions. At the same time, the bottom brush is applied to the bottom surface of the substrate. To complete the cleaning in the first cleaning station, an exit spray is used to remove/dislodge particle and metal contaminants before the wafer enters the second cleaning station for further cleaning. Next, an operation 314 moves the wafer to a second cleaning station.

In the second cleaning station, de-ionized water is again applied to the wafer through a top brush and a bottom brush in an operation 316. Surfactant solution is applied to the wafer by drip applying to the top brush. As in the first cleaning station, the top brush is lowered onto the hydrophobic layer to begin scrubbing away particle and metal contaminants from the layer surface in operation 318. The bottom brush is applied in the same way to the bottom surface of the substrate.

Next, an exit spray is used to further remove contaminants and most of the surfactant. Finally, an operation 320 performs post-cleaning operations, such as rinsing, drying and storing of the clean wafer. In operation 322, it is determined whether there are any more substrates to clean, and if there are, the method 300 repeats from operation 302. If not, the method 300 will end.

In another embodiment, the cleaning techniques of the present invention can also be used to clean other types of hydrophobic materials. Examples of these materials may be inorganic low-K dielectrics and metallization materials. Such metallization materials may include, for example, aluminum based metals, copper based metals, etc. Typically, cleaning of these exemplary materials is done after a chemical mechanical polishing operation is performed.

While this invention has been described in terms of several preferred embodiments, it will be appreciated that those skilled in the art upon reading the preceding specifications and studying the drawings will realize various alterations, additions, permutations and equivalents thereof. For example, the cleaning method described herein can be used to clean any type of
5 hydrophobic surface, whether it be in the semiconductor arts (*e.g.*, semiconductor wafers, flat panel display wafers, etc.), or other fields desiring very clean hydrophobic surfaces.

Furthermore, although a specific cleaning apparatus has been disclosed, other suitable cleaning apparatuses that implement the type of applied chemical solutions of the present invention can be used as well. It is therefore intended that the present invention includes all
10 such alterations, additions, permutations, and equivalents as fall within the true spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A method for cleaning a low K dielectric polymer surface of a semiconductor substrate, comprising:

5 applying de-ionized water and a surfactant formulation solution to the low K dielectric polymer surface to form a wettable conditioning layer, wherein the applying is configured to commence the cleaning that is targeted to remove particle and metal contaminants throughout the low K dielectric polymer surface;

10 applying de-ionized water and a surfactant solution over the low K dielectric polymer surface to continue the cleaning; and

spin-rinsing the semiconductor substrate to remove any remaining applied surfactant formulation solution or surfactant solution while removing any remaining contaminants from over the low K dielectric polymer surface.

15 2. The method of claim 1, further comprising:

switching off a flow of the surfactant formulation solution that is applied over the low K dielectric polymer surface and applying a first exit spray of de-ionized water before entering a next station.

20 3. The method of claim 2, further comprising:

switching off a flow of the surfactant solution over the low K dielectric polymer surface and applying a second exit spray of de-ionized water before entering the spin-rinsing.

25 4. The method of claim 1, wherein the surfactant formulation solution includes surfactant and a chemical enhancer.

5 5. The method of claim 4, wherein the surfactant of the surfactant formulation solution has a concentration of between about 0.1% by volume and about 1% by volume, and the chemical enhancer has a concentration of between about 0.02% by weight and about 5% by weight.

6. The method of claim 5, wherein the chemical enhancer is one of a citric acid and an ammonia, or a mixture of citric and ammonia.

10 7. The method of claim 1, wherein the surfactant solution does not include the chemical enhancer and only includes surfactant.

8. The method of claim 7, wherein the surfactant solution has a concentration of about 0.1% by volume and about 1% by volume.

15

9. The method of claim 1, wherein the low K dielectric polymer surface is an organic hydrophobic material.

20 10. The method of claim 1, wherein the applying of the de-ionized water and the surfactant formulation solution is performed in a first cleaning stage.

11. The method of claim 10, wherein the applying of the de-ionized water and the surfactant solution is performed in a second cleaning stage.

12. A method for cleaning an organic dielectric surface of a substrate, comprising:
- applying a first mixture of de-ionized water and a surfactant formulation solution to the organic dielectric surface;
- 5 scrubbing the organic dielectric surface using the first mixture;
- applying a second mixture of de-ionized water and a surfactant solution to the organic dielectric surface;
- scrubbing the organic dielectric surface using the second mixture; and
- spin-rinsing the substrate using de-ionized water to complete a removal of any
- 10 contaminants from the organic dielectric surface.

13. A method for cleaning an organic dielectric surface of a substrate as recited in claim 12, wherein the surfactant formulation solution of the first mixture includes a surfactant and a chemical enhancer.

15

14. A method for cleaning an organic dielectric surface of a substrate as recited in claim 13, wherein the surfactant has a concentration of between about 0.1% by volume and about 1% by volume, and the chemical enhancer has a concentration of between about 0.02% by weight and about 5% by weight.

20

15. A method for cleaning an organic dielectric surface of a substrate as recited in claim 12, wherein the surfactant solution of the second mixture only includes surfactant.

16. A method for cleaning an organic dielectric surface of a substrate as recited in
- 25 claim 15, wherein the surfactant has a concentration of between about 0.1% by volume and

about 1% by volume.

17. A method for cleaning an organic dielectric surface of a substrate as recited in claim 12, wherein the applying of the first mixture of the de-ionized water and the surfactant formulation solution to the organic dielectric surface is performed through the use of a first brush cleaning stage that is configured to perform the scrubbing of the organic dielectric surface.

18. A method for cleaning an organic dielectric surface of a substrate as recited in claim 17, wherein the applying the first mixture further comprises:

drip applying the surfactant formulation solution to a top brush of the first brush cleaning stage.

19. A method for cleaning an organic dielectric surface of a substrate as recited in claim 12, wherein the applying of the second mixture of the de-ionized water and the surfactant solution to the organic dielectric surface is performed through the use of a second brush cleaning stage that is configured to perform the scrubbing of the organic dielectric surface.

20. A method for cleaning an organic dielectric surface of a substrate as recited in claim 19, wherein the applying the second mixture further comprises:

drip applying the surfactant solution to a top brush of the second brush cleaning stage.

21. A wafer cleaning apparatus for cleaning an organic dielectric surface, comprising:

a first cleaning stage for applying a first mixture of de-ionized water and a surfactant formulation solution to the organic dielectric surface, the first cleaning stage having a first brush system for scrubbing the organic dielectric surface using the first mixture;

5 a second cleaning stage for applying a second mixture of de-ionized water and a surfactant solution to the organic dielectric surface, the second cleaning stage having a second brush system for scrubbing the organic dielectric surface using the second mixture; and

a spin-rinsing bowl for rinsing the wafer using de-ionized water to complete a removal of any contaminants from the organic dielectric surface.

10 22. A wafer cleaning apparatus as recited in claim 21, wherein the surfactant formulation solution of the first mixture includes a surfactant and a chemical enhancer.

23. A wafer cleaning apparatus as recited in claim 22, wherein the surfactant has a concentration of between about 0.1% by volume and about 1% by volume, and the chemical
15 enhancer has a concentration of between about 0.02% by weight and about 5% by weight.

24. A wafer cleaning apparatus as recited in claim 21, wherein the surfactant solution of the second mixture only includes surfactant.

20 25. A wafer cleaning apparatus as recited in claim 24, wherein the surfactant has a concentration of between about 0.1% by volume and about 1% by volume.

26. A method for cleaning a surface of a semiconductor substrate, comprising:

applying de-ionized water and a surfactant formulation solution to the surface to form
25 a wettable conditioning layer, wherein the applying is configured to commence the cleaning

that is targeted to remove particle and metal contaminants throughout the surface;

applying de-ionized water and a surfactant solution over the surface to continue the cleaning; and

5 spin-rinsing the semiconductor substrate to remove any applied surfactant formulation solution or surfactant solution while removing any remaining particle contaminants from over the surface.

27. A method for cleaning a surface of a semiconductor substrate as recited in claim 26, wherein the surface is composed of material regions of one or more of an organic
10 dielectric material region, an inorganic dielectric material region, and a metallization material region.

28. A method for cleaning a surface of a semiconductor substrate as recited in claim 26, wherein the metallization material region is selected from a group consisting of an
15 aluminum based metal, and a copper based metal.

29. A method for cleaning a surface of a semiconductor substrate as recited in claim 26, further comprising:

applying a chemical enhancer to the surfactant solution in order to convert the
20 surfactant solution into a second surfactant formulation solution.

30. A method for cleaning a surface of a substrate, comprising:

applying a first mixture of de-ionized water and a surfactant formulation solution to the surface;

25 scrubbing the surface using the first mixture;

applying a second mixture of de-ionized water and a surfactant solution to the surface;
scrubbing the surface using the second mixture; and
spin-rinsing the surface of the substrate using de-ionized water to complete a removal
of any contaminants from the surface.

5

31. A method for cleaning a surface of a substrate as recited in claim 30, wherein
the surface is one of an organic low-k dielectric surface and an inorganic low-k dielectric
surface.

10 32. A method for cleaning a surface of a substrate as recited in claim 30, wherein
the surface has metallization regions.

33. A method for cleaning a surface of a substrate as recited in claim 30, wherein
the metallization regions are aluminum and copper based.

15

34. A method for cleaning a surface of a substrate as recited in claim 30, wherein
the applying of the second mixture of de-ionized water and a surfactant solution to the surface
further comprises:

20 applying a chemical enhancer to the surfactant solution to convert the surfactant
solution into a surfactant formulation solution.

35. A method for cleaning a surface of a substrate, comprising:

applying a surfactant solution to the surface;

scrubbing the surface; and

spin-rinsing the surface of the substrate using de-ionized water to complete a removal of any contaminants from the surface.

36. A method for cleaning a surface of a substrate as recited in claim 35, further
5 comprising:

mixing a chemical enhancer with the surfactant solution to produce a surfactant formulation solution that is applied to the surface.

37. A method for cleaning a surface of a substrate as recited in claim 36, wherein
10 the scrubbing is performed using a brush system.

38. A method for cleaning a surface of a substrate as recited in claim 37, wherein
the brush system is configured to clean with the surfactant formulation while a de-ionized
water source is applied to the brush system using a TTB application technique.

15

39. A method for cleaning a surface of a substrate as recited in claim 35, wherein
the surface is one of an organic low-k dielectric surface and an inorganic low-k dielectric
surface and a metallic surface, or a combination thereof.

20 40. A method for cleaning a surface of a substrate as recited in claim 35, further
comprising:

applying the surfactant solution using a TTB application technique.

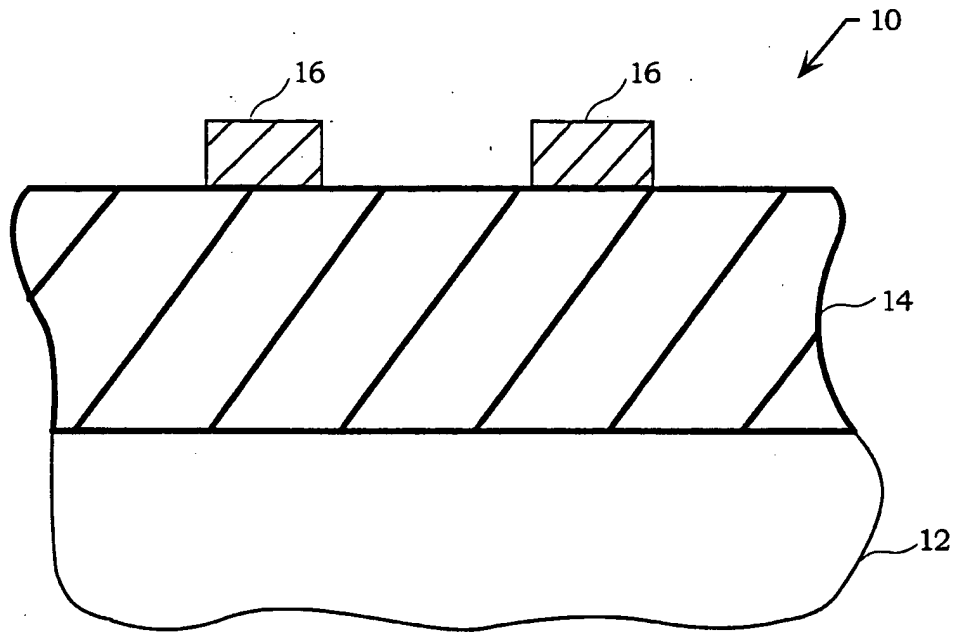


FIG. 1A

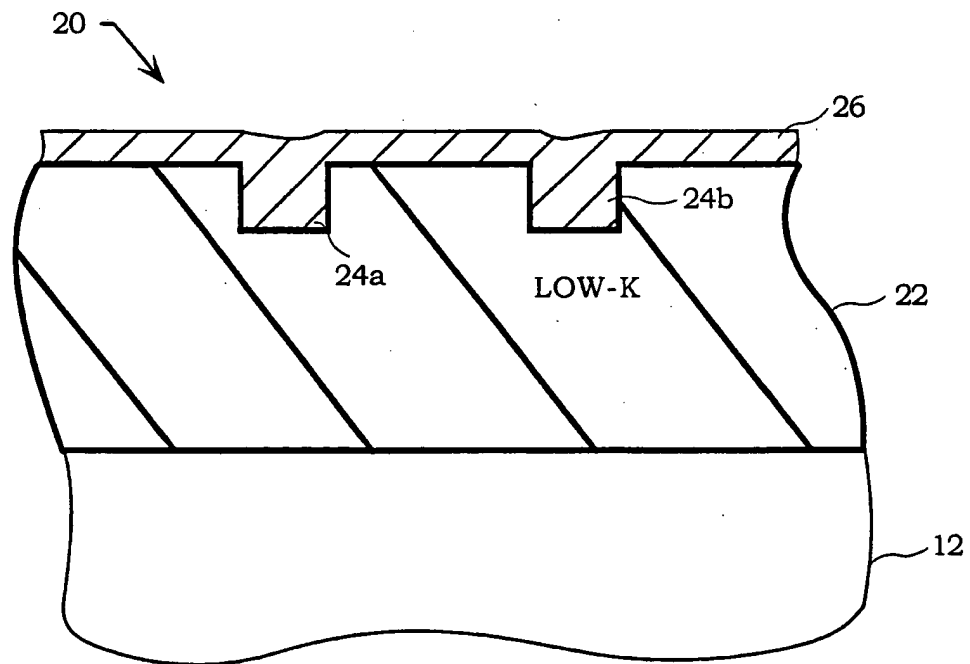


FIG. 1B

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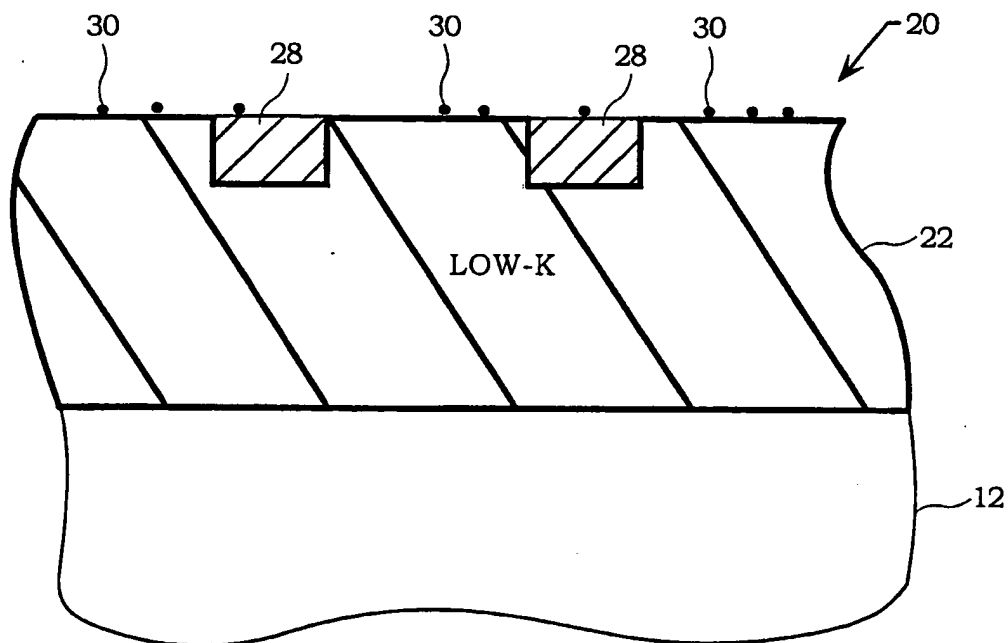


FIG. 1C

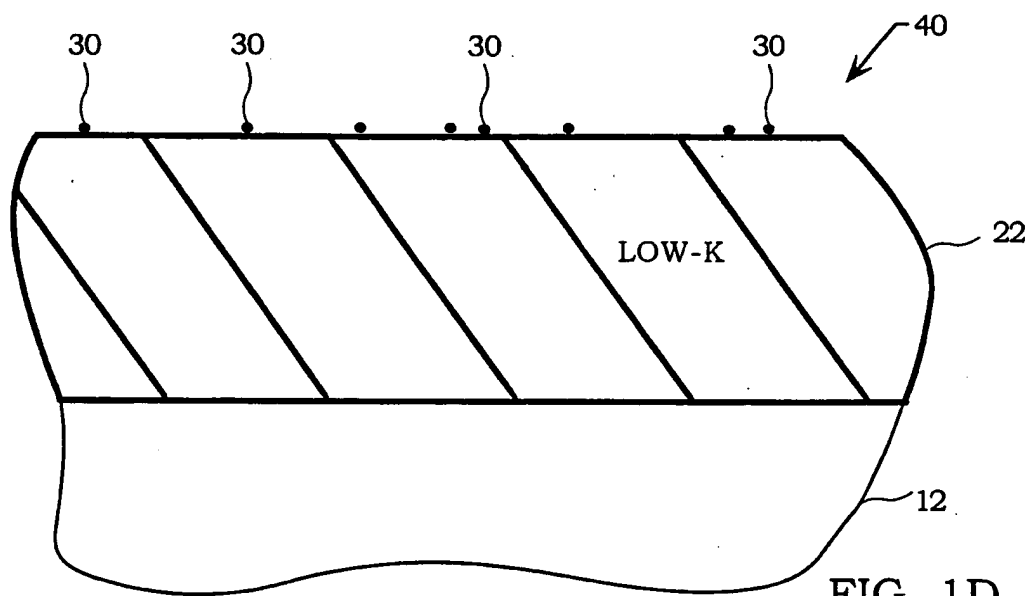


FIG. 1D

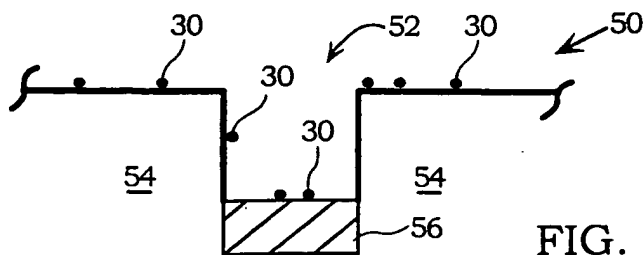


FIG. 1E

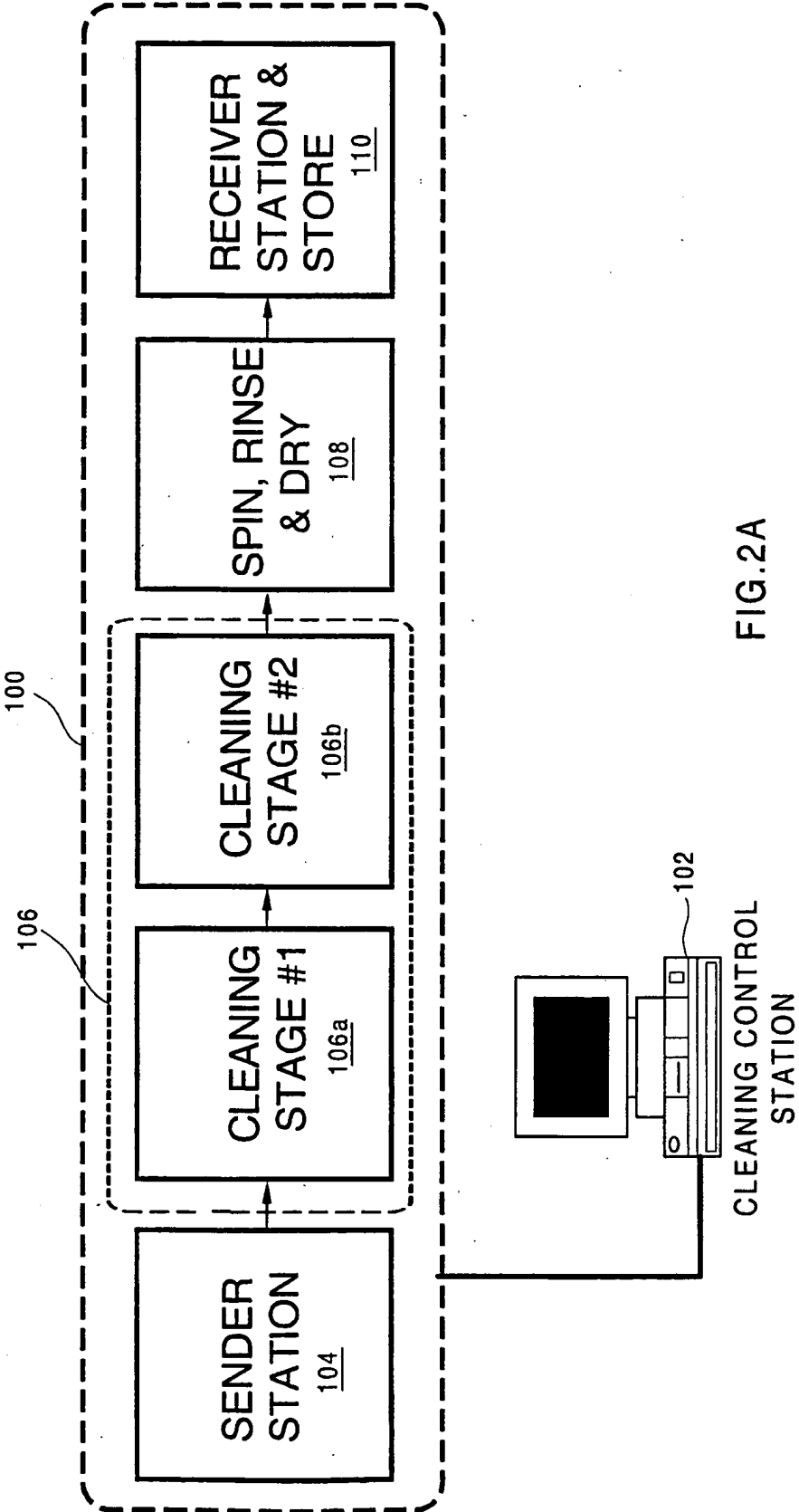


FIG. 2A

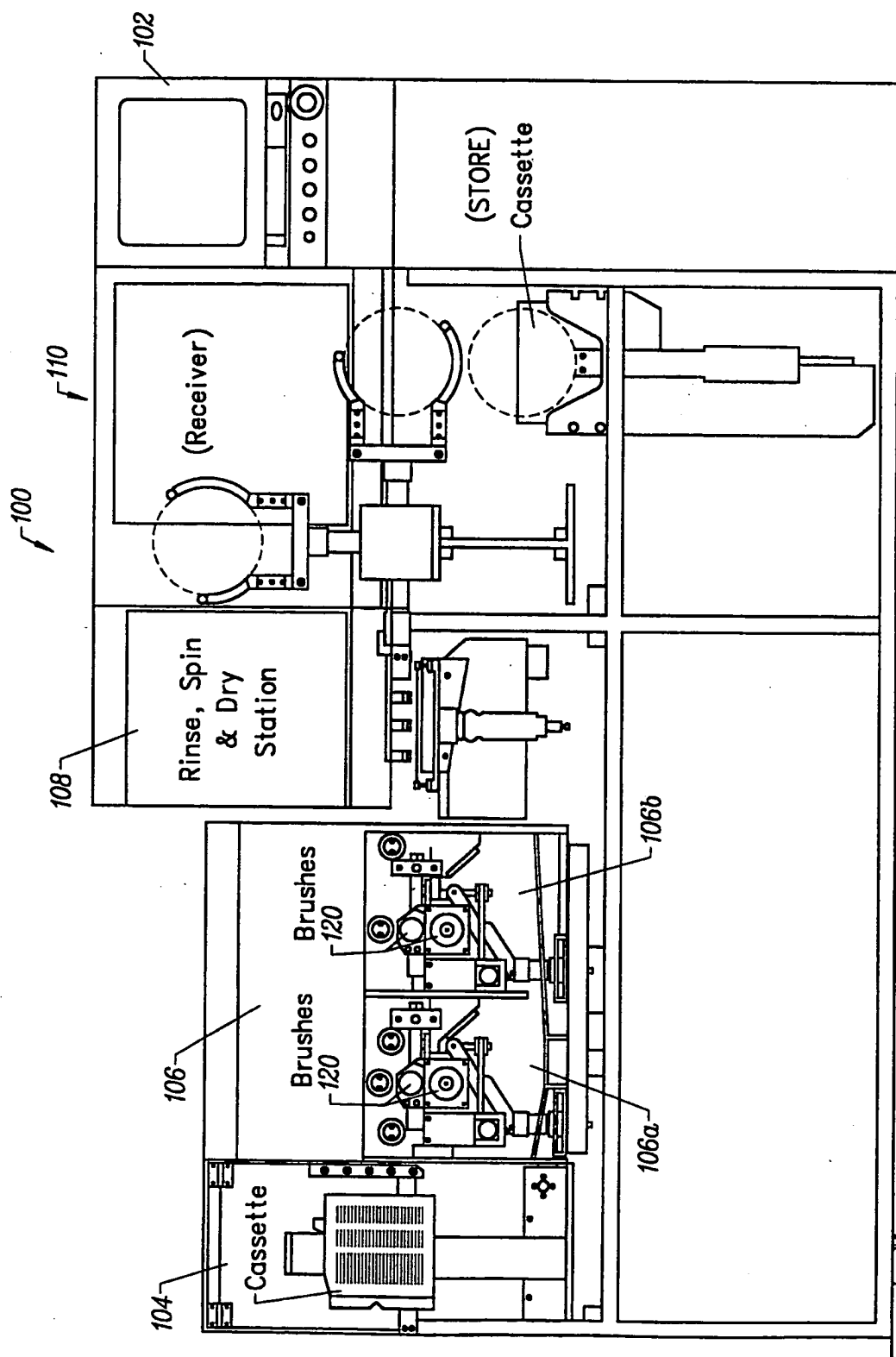
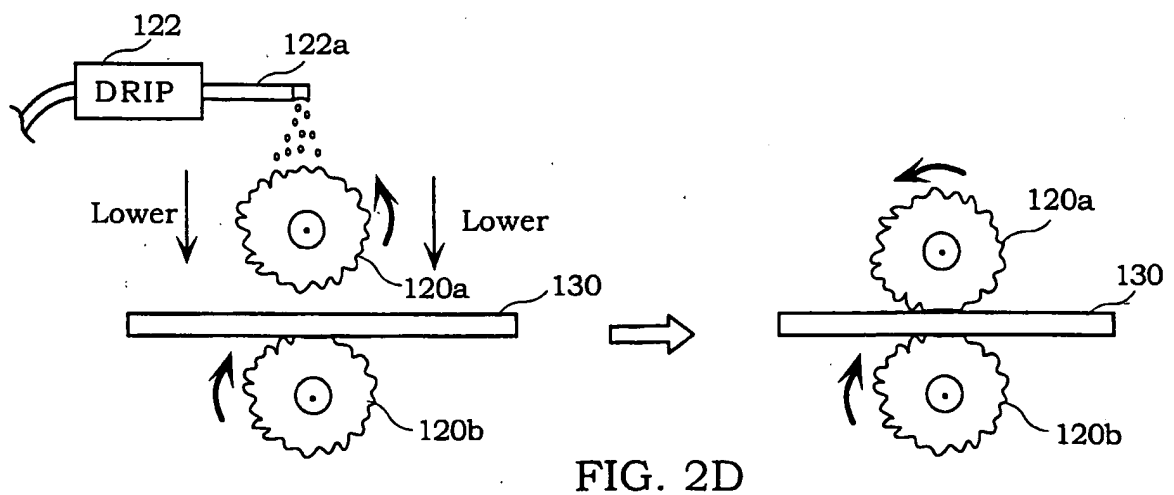
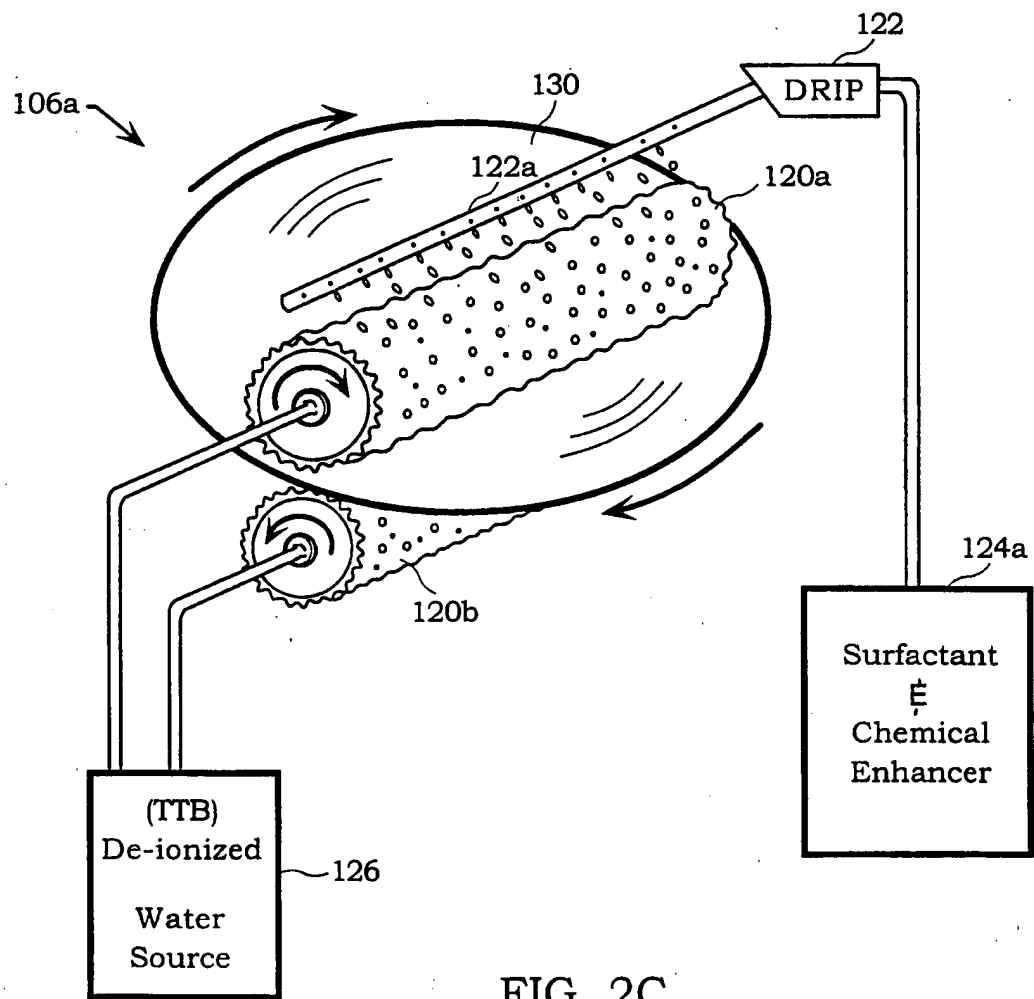


FIG. 2B



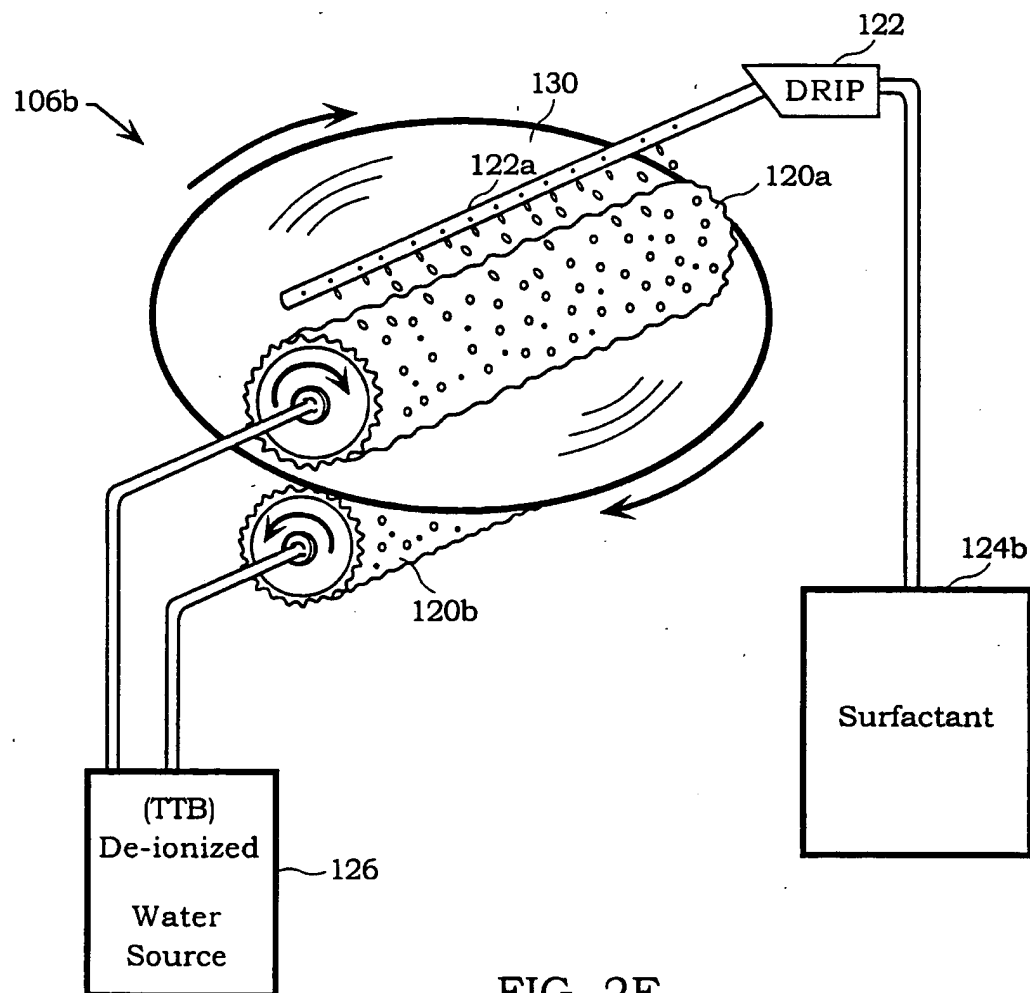


FIG. 2E

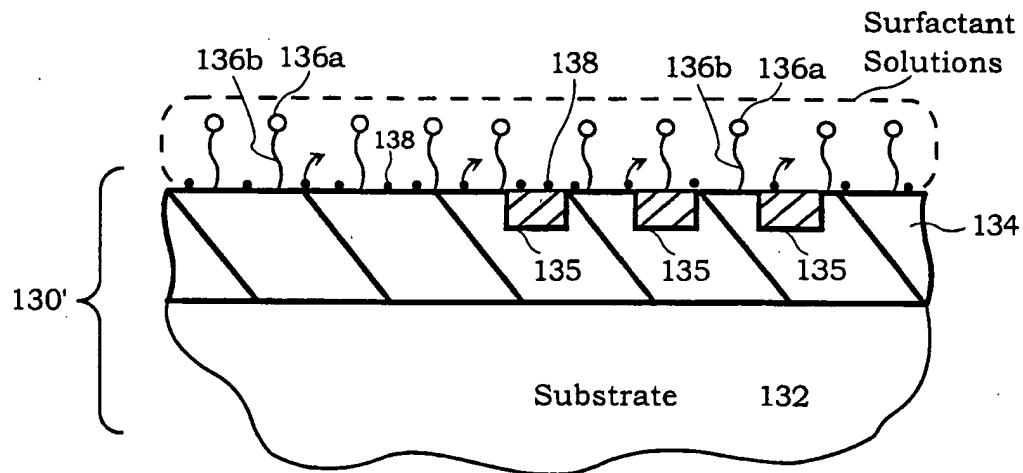


FIG. 3A

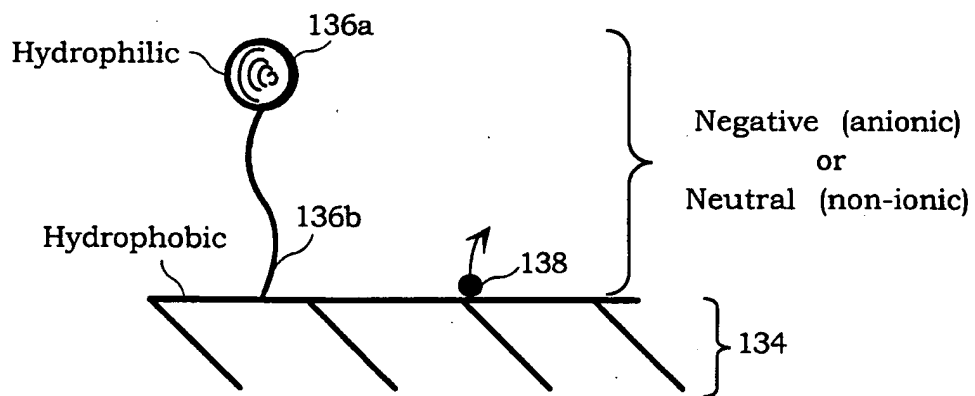


FIG. 3B

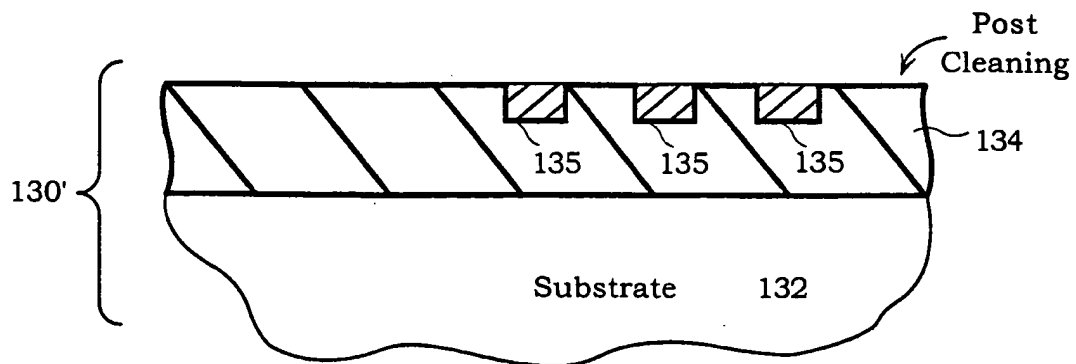


FIG. 3C

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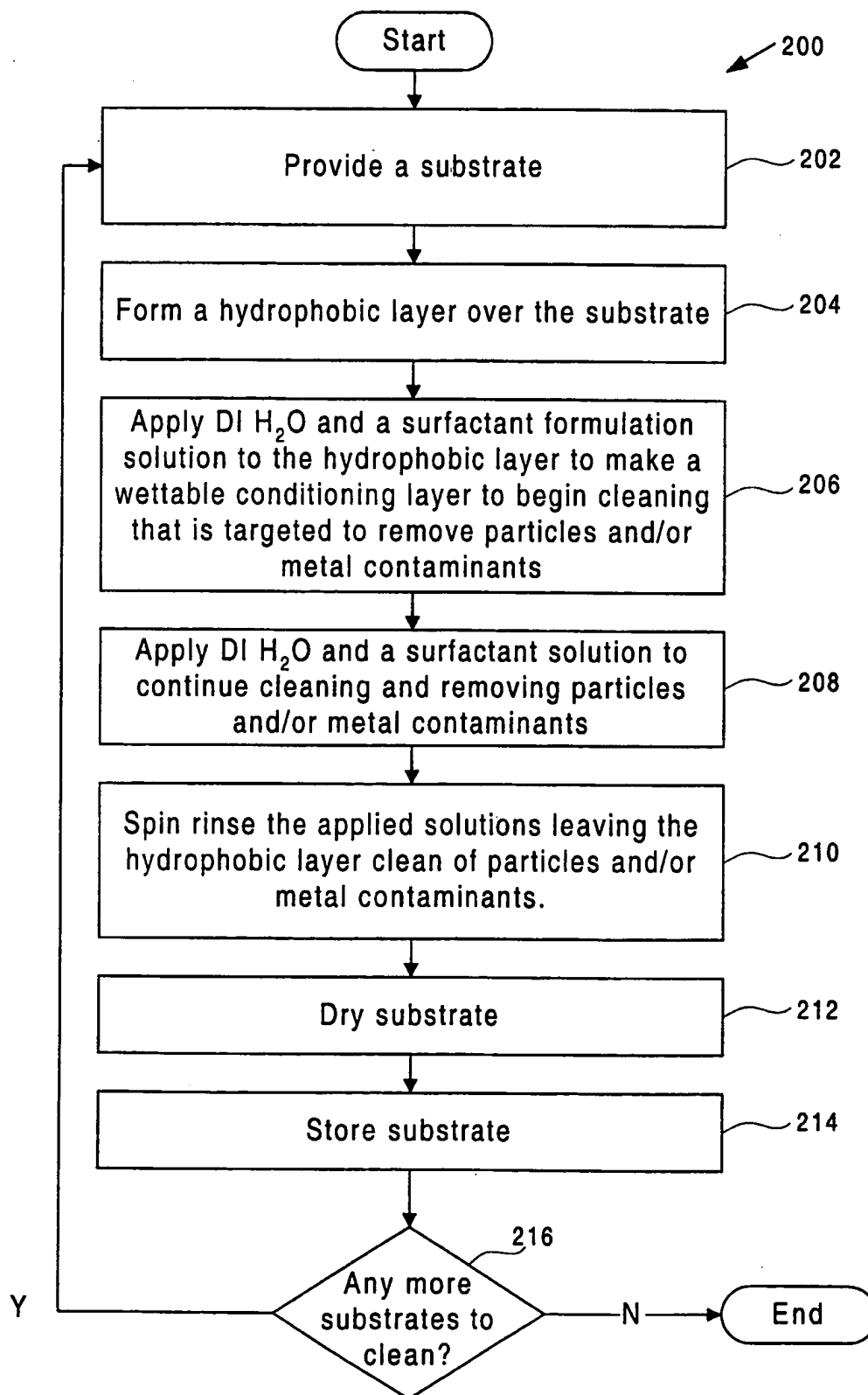


Fig. 4

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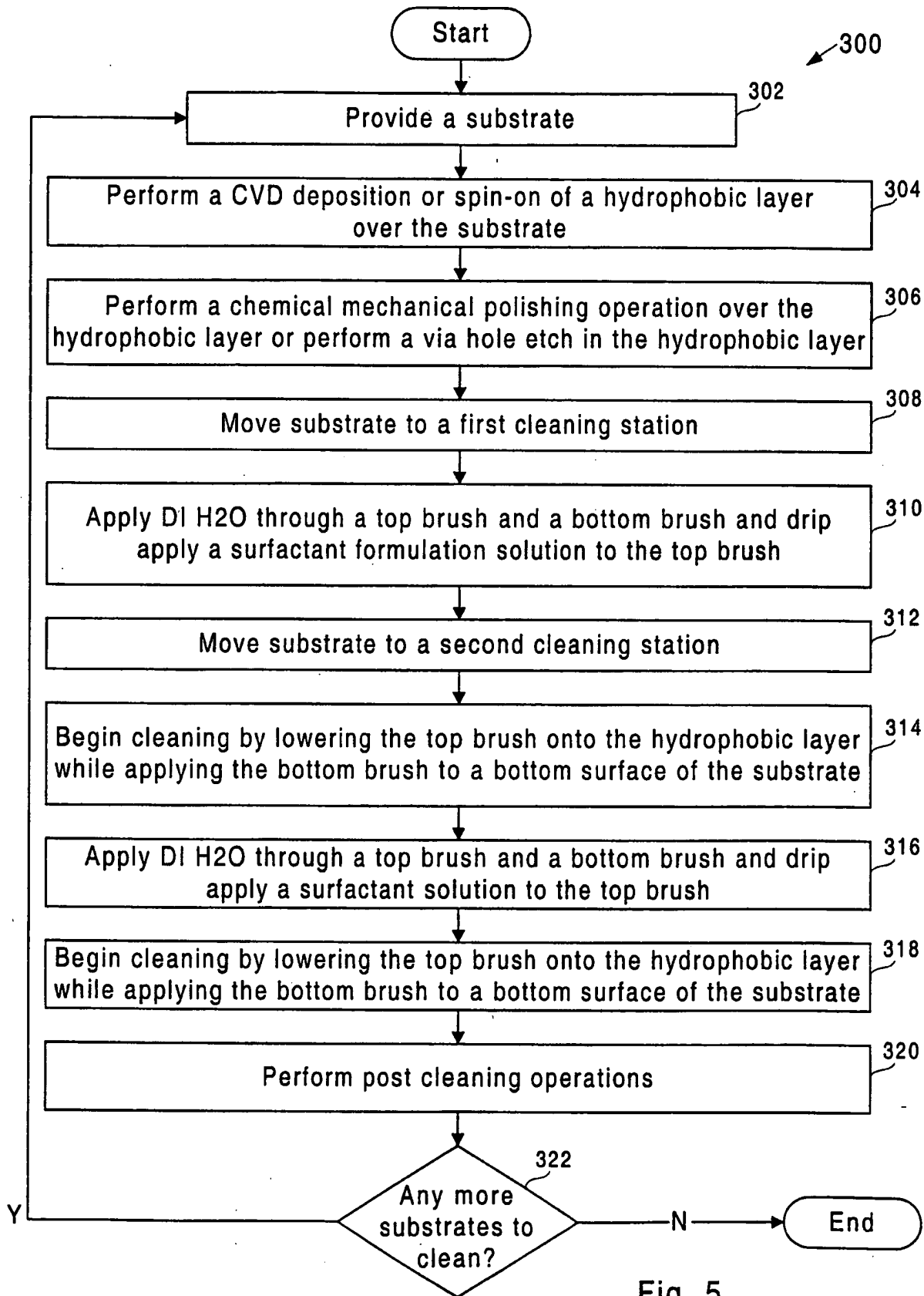


Fig. 5

International Application No

PCT 'S 99/19634

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 B08B3/08 B08B1/04 H01L21/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 B08B H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	FR 2 722 511 A (ONTRAK SYSTEMS, INC.) 19 January 1996 (1996-01-19)	1,4,7, 9-11, 26-28, 35-40
A	abstract page 8, line 6 -page 10, line 6 page 12, line 8 -page 14, line 5 page 15, line 1 - line 17 page 16, line 9 -page 17, line 35; figures --- -/--	2,3,5-7, 12-15, 17-24, 30-33

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

'&' document member of the same patent family

Date of the actual completion of the international search

18 January 2000

Date of mailing of the international search report

24 01 2000

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Authorized officer

Van der Zee, W

INTERNATIONAL SEARCH REPORT

International Application No

PCT '93 99/19634

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
(WO 97 13590 A (ONTRAK SYSTEMS, INC. ET AL) 17 April 1997 (1997-04-17)	12,13, 15,17, 19,21, 22,24, 26,27, 30,31, 35-40
A	abstract page 3, line 23 -page 5, line 30 page 6, line 23 -page 7, line 13 page 8, line 18 - line 29; figures	
A	--- US 5 129 955 A (TANAKA) 14 July 1992 (1992-07-14)	1,4,6,7, 9-11,28, 32,33
A	abstract column 4, line 52 -column 6, line 68; figures 2,6	1,4,6, 9-13,21, 22,26, 27,30, 31,35, 36,39
A	--- PATENT ABSTRACTS OF JAPAN vol. 12, no. 207 (E-621), 14 June 1988 (1988-06-14) -& JP 63 004617 A (MITSUBISHI ELECTRIC CORP.), 9 January 1988 (1988-01-09)	1,4, 9-13,21, 22,26, 27,30, 31,35, 36,39
	abstract -----	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/IS 99/19634

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
FR 2722511 A	19-01-1996	DE 19525521 A JP 8187475 A	21-03-1996 23-07-1996
-----	-----	-----	-----
WO 9713590 A	17-04-1997	AU 7264596 A EP 0914216 A US 5868863 A US 5858109 A US 5806126 A	30-04-1997 12-05-1999 09-02-1999 12-01-1999 15-09-1998
-----	-----	-----	-----
US 5129955 A	14-07-1992	JP 2275631 A KR 9301287 B	09-11-1990 25-02-1993
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JP 63004617 A	09-01-1988	NONE	
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